

**Remarks/Arguments:**

Claims 1, 2 and 5-16 were rejected under 35 U.S.C. § 102(b) as anticipated by Weisfield (U.S. Patent No. 6,856,351). Claims 3 and 4 were rejected under 35 U.S.C. § 103(a) as obvious over Weisfield and Takada et al. (U.S. Pub. No. 2001/0015404). Claims 18 and 19 were rejected under 35 U.S.C. § 103(a) as obvious over Weisfield. Claims 17 and 20 were indicated as allowable if re-written in independent form. It is respectfully submitted, however, that the claims are patentable over the art of record for the reasons set forth below.

Applicants' invention, as recited by claim 1, includes a feature which is neither disclosed nor suggested by the art of record, namely:

a bias circuit operable to apply voltage across the pixels to forward bias the photodiode regions during a step selected from the group consisting of a reset step for each pixel or a charge blanking step for each pixel (emphasis added).

This feature is supported by the originally filed application at page 7, lines 3-5 and 21-25. No new matter has been added.

Weisfield is directed to a method for reducing image lag and blooming in image sensor arrays. The method includes use of a clamping diode 212 to maintain a photodiode 216 under reverse bias, even when subject to high levels of illumination. See col. 4, lines 28-32. While Weisfield does state "[t]o accommodate any excess current, diode 312 may switch into forward bias of about 0.1V." it is noted that diode 312 is not the photodiode, the photodiode is diode 316. Accordingly, this statement does not meet the limitations of claims 1 and 18. The embodiment disclosed in Applicants' claim 1, on the other hand, recites forward biasing the photodiode during either a reset step or a charge blanking step for each pixel. Because Weisfield discloses that the photodiode is always under reverse bias, Weisfield can not and does not disclose "forward bias[ing] the photodiode regions during a step selected from the group consisting of a reset step for each pixel or a charge blanking step for each pixel," as required.

Takada is directed to a solid state imaging device that uses phototransistors as photosensitive elements. The Examiner argues that Takada discloses forward biasing the phototransistor during a reset step, citing to Takada at paragraphs 256-258.

Of paragraphs 256-258, only paragraph 258 describes the phototransistor receiving a forward bias. There is no description in paragraph 258, however, about the forward bias being applied during a reset step, nor is there any description about it being applied during a charge blanking step. Applicants assume, from the citation to paragraphs 256-257, that the Examiner is referring to the heading "(2-b) Reset Operation." Paragraph 258, which describes the forward bias operation, does not fall under the "Reset Operation" heading. Instead, it falls

under a separate heading reading "When the Signal  $\Phi$ RL is Kept at the Fifth Voltage." Furthermore, Takeda discloses forward biasing a *phototransistor* not a *photodiode* as required by the claims of the subject invention, and, the stated purpose of forward biasing this phototransistor is to keep the transistor T10 turned on (See Takeda paragraph 258). There is no similar structure to the transistor T10 in example apparatus described in the subject specification. Thus, Takada does not disclose "forward bias[ing] the photodiode regions during a step selected from the group consisting of a reset step for each pixel or a charge blanking step for each pixel," as required.

As set forth above, Takeda discloses a radically different pixel structure than the subject invention. The Examiner has not stated a reason, independent of Applicant's disclosure, why a person of ordinary skill in the art would modify Takeda to meet the limitations of the subject invention or even how such a modification would be accomplished as so do so would require replacing the phototransistor with a photodiode. Without such a statement, there is no substantial evidence to support the combination of Weisfield and Takeda.

Accordingly, claim 1 is patentable over the art of record. Claim 18, while not identical to claim 1, includes a feature similar to that recited in claim 1. Accordingly, claim 18 is also patentable over the art of record for the reasons set forth above.

Claims 5-6 and 8-17 include all the features of claim 1 from which they depend and claim 20 includes all the features of claim 18 from which it depends. Accordingly, claims 5-6, 8-17 and 20 are also patentable over the art of record for the reasons set forth above.

In view of the foregoing amendments and remarks, Applicants request that the Examiner reconsider and withdraw the rejections of claims 1, 5-6, 8-18 and 20.

Respectfully submitted,

  
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